US-PAT-NO: 6333532

DOCUMENT-IDENTIFIER: US 6333532 B1

TITLE: Patterned SOI regions in semiconductor chips

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Detailed Description Text - DETX (2):
Referring now to the drawing, FIG. 1 shows an SOI structure 10 having a substrate 12 of a poly or single crystalline semiconductor material containing Si such as Si alone, SiGe, **SiC,** with a major upper surface 13. On major surface 13, a dielectric mask 14 is formed. Dielectric mask 14 may be of a material such as SiO.sub.2, Si.sub.3 N.sub.4, **polysilicon,** diamond-like-carbon, Al.sub.2 O.sub.3 or combinations thereof. Dielectric mask 14 is lithographically patterned to form openings 15 and 15'. Mask 14 may be formed with one or more patterned dielectric layers.

Detailed Description Text - DETX (19):
In place of a single trench 94, a plurality of trenches 94 may be formed side by side parallel to one another such as where trench 35 is located to remove dislocations and to provide electrical isolation. Trench or trenches 94 may have their respective sidewalls and bottom oxidized to form an insulator such as SiO.sub.2 and filled with an **oxide or a polysilicon**. Selective placement of trenches 94 may also provide thermal dissipation from layer 29 or the top of substrate 12 to substrate 12 below. To increase thermal conductivity, trench 94 may be filled with a thermally conductive material such as a conductive oxide, metal or doped **polysilicon**.

Detailed Description Text - DETX (20):
Referring to FIG. 9, a decoupling capacitor 102 is shown formed in substrate 12 in bulk semiconductor region 38 of substrate 12 which may be adjacent one or more patterned SOI regions 18. A trench 104 is formed in upper surface 13 in substrate 12. The sidewalls 105 and bottom 106 of trench 104 are covered by a layer of dielectric 108 such as silicon dioxide, silicon nitride or combinations thereof. Trench 104 may be filled with a conductive material 109 such as p+ or n+ doped **polysilicon** or a metal. The top surface of conductive material 109 may be planarized to be, for example, coplanar with surface 13 by chemical mechanical processing (CMP).

Detailed Description Text - DETX (21):

Referring to FIG. 10, a decoupling capacitor 112 is shown formed in substrate 12 in a bulk semiconductor region 18 of substrate 12 which may be adjacent one or more patterned SOI regions 38. A trench 114 is formed in upper surface 13 in substrate 12. The sidewalls 115 and bottom 116 of trench 114 and surface 13 are covered by a layer of dielectric 118 such as silicon dioxide, silicon nitride or combinations thereof. Trench 114 may be filled with a conductive material 119 such as p+ or n+ doped **polysilicon** or a metal. The top surface of conductive material 119 may be planarized to be, for example, coplanar with the top surface of dielectric 118 by a process such as CMP.

Detailed Description Text - DETX (22):

Referring to FIG. 11, a body contact 120 for field effect transistors 28 shown in FIGS. 2B and 8 is shown by making electrical contact between layer 29 and substrate 12 below buried oxide layer 17. A trench 122 is formed from surface 13 through layer 29, through buried oxide layer 17 and into substrate 12. Trench 122 may have a dielectric layer 124 on sidewalls 125 from the bottom of sidewall 125 to the upper surface 126 of buried oxide layer 17. Trench 122 may be filled with conductive material 119 such as a conductive oxide, p+ or n+ **polysilicon** or metal.

Detailed Description Text - DETX (23):

Referring to FIG. 12, a body contact 130 for field effect transistors 28 shown in FIGS. 2B and 8 is shown by making electrical contact between layer 29 and substrate 12 below buried oxide layer 17. A trench 132 is formed from surface 13 through layer 29, through buried oxide layer 17 and into substrate 12 for a predetermined depth. Trench 132 has sidewalls 135. Trench 132 may be filled with a conductive material 129 such as a conductive oxide, p+ or n+ **polysilicon** or metal.

Claims Text - CLTX (23):

8. The semiconductor structure of claim 7 wherein said semiconductor substrate is selected from the group consisting of SiGe and **SiC**.

Claims Text - CLTX (43):

19. The semiconductor structure of claim 17 wherein said trench is filled with a material selected from the group consisting of p+ **polysilicon,** n+ **polysilicon** and a metal.

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See image for Certificate of Correction

TITLE: Metallic oxide gate electrode stack having a metallic gate dielectric metallic gate electrode and a metallic arc layer

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Brief Summary Text - BSTX (5):

In modern semiconductor device manufacturing, a plurality of layers are generally deposited on a semiconducting substrate, that is typically made of silicon. These layers are then patterned and etched by photolithography and etch techniques to form a gate electrode stack. Generally, the gate electrode stack includes a gate dielectric overlying a substrate channel region, a **polysilicon** (poly) gate layer overlying the gate dielectric, and an anti-reflective coating (ARC) layer overlying the gate layer which is typically silicon nitride. Following deposition of these three basic layers (i.e., gate dielectric, gate electrode, and ARC), a photoresist layer is spun onto the substrate over the top of the ARC layer. The photoresist is then selectively exposed to light through a lithographic mask to form exposed and unexposed regions of the photoresist. The exposed photoresist regions are then developed and removed from the substrate, thereby exposing top portions of the ARC layer. The exposed portions of the ARC layer are then exposed to an etch process which removes portions of the ARC layer, then removes portions the gate layer, and/or finally removes portions of the gate dielectric. This removal defines the gate stack structure.

Brief Summary Text - BSTX (7):

In order to reduce the magnitude of these problems, anti-reflective coating (ARC) layers were developed for MOS manufacturing. Several different ARC layers have typically been used in order to prevent or largely suppress unwanted reflection of the energy during photoresist exposure. ARC layers such as silicon nitride, silicon oxynitride, silicon-rich silicon nitride, and silicon-rich silicon oxynitride, have been used as an ARC layer in connection with **polysilicon** MOS gate structures. While such ARC layers have been largely successful in suppressing unwanted reflection in **polysilicon** gate structures, problems have been encountered with the use of these known ARC materials. The

problems include high stress associated with the ARC layers, poor adhesion between the ARC layer and gate electrodes, and the need for high deposition temperatures which is generally undesirable in the IC industry. The relatively high stress and low adhesion of the ARC layer results in peeling or delamination of the ARC layer from the poly gate layer, which substantially impacts device yield. In an attempt to improve device yield, it is generally desirable to put an adhesive "glue" layer between the ARC layer and the **polysilicon** gate layer which increases process complexity, reduces wafer throughput and IC time to market, and may adversely increase gate resistance.

Brief Summary Text - BSTX (8):

As modern semiconductor manufacturing moves toward use of metal gate layers rather than **polysilicon** gate layers, problems with efficacy and integration of silicon nitride, silicon oxynitride, and like ARC layers become even more pronounced. Indeed, it has been found that the conventional silicon nitride and silicon oxynitride groups of materials cannot adhere properly to metal gates, such as TaN, TiN, or W.sub.2 N, and may adversely chemically interact with the underlying **polysilicon** material.

Detailed Description Text - DETX (3):

Generally, FIGS. 1-6 herein teach a process for forming a metallic gate stack structure useful for making metallic-gate metal oxide semiconductor (MOS) transistors or metallic-gate complementary MOS (CMOS) transistor structures. The metallic gate stack is preferable formed to contain a bottom metallic gate dielectric (e.g., TiO.sub.2, Ta.sub.2 O.sub.5, or composites thereof), followed by an intermediate metallic conductive gate electrode (e.g., TaN), followed by a top layer of one of either a metal oxide, metal silicon oxide, metal silicon nitride, or metal silicon oxynitride anti-reflective coating (ARC) layer (e.g., TaSi.sub.y O.sub.z N.sub.t or Ta.sub.2 O.sub.5). These stacked materials are etched to form the metallic gate stack by utilizing a fluorine-chlorine-fluorine time-serial plasma or reactive ion etch (RIE) sequence. The resulting metallic stack has a metallic dielectric layer that is improved over conventional silicon dioxide since it can be formed thicker whereby leakage current is reduced while still maintaining an equivalent SiO.sub.2 thickness of roughly 10-50 Angstroms to preserve transistor performance. The tantalum-based metallic gate electrode provides improved transistor performance and has improved conductivity over conventional **polysilicon** gates. In addition, **polysilicon** gates will react with metallic oxides creating SiO.sub.2 which adversely affect the overall .epsilon. value of the gate dielectric and affects the thickness of the gate dielectric in a manner that is difficult to control. Most importantly, the tantalum-based ARC layer provides greater adhesion to the metal gate whereby MOS yield is

improved, eliminates the need for a resistive or complex glue layer, reduces gate stack stress in the integrated circuit (IC), and may be formed at lower temperatures that are more compatible with deep submicron devices (gate dimensions less than 0.25 microns).

Detailed Description Text - DETX (4):

In FIG. 1, a semiconductor device 10 is provided. Device 10 has a substrate 12. The substrate 12 may be provided as any known substrate material, such as intrinsic or compensated silicon, doped silicon, silicon-on-insulator (SOI) wafers, germanium, gallium arsenide (GaAs), **silicon carbide,** epitaxial regions, etc.. Device 10 contains trench isolation regions. A trench region is formed by selectively reactive ion etching (RIE) into portions of the substrate to form trench regions. These trench regions are then lined with a liner layer 14. The liner 14 is typically formed by wet and/or dry thermal oxidation whereby the liner 14 is preferably silicon dioxide (SiO.sub.2) or some composite thereof. The dielectric trench fill 16 in FIG. 1 is typically formed by chemical vapor deposition (CVD) of tetraethylorthosilicate (TEOS) that is subsequently planarized by a chemical mechanical polishing (CMP) process and/or a resist etch back (REB) process. Although trench isolation (e.g., shallow trench isolation (STI)) is specifically shown in FIG. 1, the trench isolation in FIG. 1 may be replaced with other isolation schemes such as local oxidation of silicon (LOCOS), **polysilicon** buffer LOCOS (PBL), field shield isolation, and the like.

Detailed Description Text - DETX (7):

Further, according to the present invention, a metal gate layer 20 is deposited on gate dielectric 18. The metal gate layer 20 may be formed of any one of more metallic materials, including titanium, molybdenum, tantalum, platinum, iridium, tungsten, titanium nitride (TiN), tungsten nitride (WN), other metallic nitrides, composites thereof, or the like. A tantalum or titanium based gate electrode is preferred herein. Metal gates are now preferred in the IC industry over **polysilicon** gates since metal gates offer greater conductivity for improved integrated circuit (IC) performance. Metal gates also do not charge deplete via depletion regions to the extent that **polysilicon** layers deplete, whereby the effective thickness of the gate dielectric does not change as much, if at all, with applied gate voltages. Since the gate layer 20 contains metallic atoms to serve this performance improvement purpose, it is preferable that the gate dielectric 18 formed with a metallic dielectric rather than SiO.sub.2 for integration purposes a well as performance purposes. The metal gate layer 20 may be formed by chemical vapor deposition (CVD) or low power physical vapor deposition (PVD). Typically, the metal gate layer is on the order of 1000 to 4000 angstroms in thickness,

although other thicknesses are possible depending upon the application.

Detailed Description Text - DETX (9):

According to a particular embodiment of the present invention, the gate dielectric 18, metal gate layer 20, and ARC layer 22 all contain the same metallic atom, such as tantalum, which enables formation of all three layers 18, 20, and 22 in the same semiconductor tool or chamber without breaking vacuum. When performing this insitu gate stack formation, the gate dielectric will be formed of tantalum pentoxide which is optionally doped with one or more silicon and/or nitrogen, the metal gate layer is then formed from tantalum nitride or a like tantalum-based material, and the ARC layer is tantalum pentoxide that is also optionally doped with one or more of silicon and/or nitrogen. Accordingly, the present invention provides an advantage of forming all three tantalum-based layers insitu in a single semiconductor tool having one or more processing chambers. This insitu process is unlike the prior art which typically forms a silicon dioxide gate dielectric, a **polysilicon** gate layer, and a nitride ARC layer, where each layer requires different deposition techniques, source materials/gases, and semiconductor equipment. This insitu process is especially advantageous since metallic gates will oxidize in an air ambient if removed from a processing tool without a capping layer (e.g., the ARC layer). As is clear from FIG. 1, layers 18, 20, and 22 are all initially blanket deposited.